

What is claimed is:

1 1. A fabrication method for a damascene bit line
2 contact plug, comprising the steps of:
3 providing a semiconductor substrate having a first gate
4 conductive structure, a second gate conductive
5 structure and a source/drain region, in which the
6 source drain region is formed in the substrate
7 between the first gate conductive structure and
8 the second gate conductive structure;
9 forming a first conductive layer in a space between the
10 first gate conductive structure and the second
11 gate conductive structure, in which the first
12 conductive layer is electrically connected to the
13 source/drain region;
14 forming an inter-layer dielectric with a planarized
15 surface overlying the substrate to cover the
16 first conductive layer, the first gate conductive
17 structure, and the second gate conductive
18 structure;
19 forming a bit line contact hole in the inter-layer
20 dielectric to expose the top of the first
21 conductive layer; and
22 forming a second conductive layer in the bit line
23 contact hole, in which the combination of the
24 second conductive layer and the first conductive
25 layer serves as a damascene bit line contact
26 plug.

1 2. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 1, wherein the formation of
3 the first conductive layer comprises the steps of:

4 forming a first liner to covering the first gate
5 conductive structure, the second gate conductive
6 structure and the substrate;

7 providing a first photoresist layer having an opening
8 corresponding to the bit line contact hole;

9 removing the first liner exposed within the opening to
10 expose the source/drain region located between
11 the first gate conductive structure and the
12 second gate conductive structure;

13 removing the first photoresist layer;

14 depositing the first conductive layer to fill the space
15 between the first gate conductive structure and
16 the second gate conductive structure;

17 performing a chemical mechanical polishing process on
18 the first conductive layer, in which the top of
19 the first conductive layer is higher or
20 approximately equal to the first liner positioned
21 on top of the first gate conductive structure and
22 the second gate conductive structure;

23 providing a second photoresist layer having a pattern
24 corresponding to the bit line contact hole; and

25 removing the first conductive layer not covered by the
26 second photoresist layer, in which the first
27 conductive layer remains in the space between the
28 first gate conductive structure and the second

29 gate conductive structure and is electrically
30 connected to the source/drain region.

1 3. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 2, wherein the formation of
3 the first conductive layer further comprises the steps of:
1 removing the second photoresist layer; and
2 performing a wet etching process to remove polymer
3 residue from the substrate.

1 4. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 2, wherein the first liner
3 is SiN or SiON.

1 5. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 2, wherein the thickness of
3 the first liner is 100~120Å.

1 6. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 1, wherein the formation of
3 the bit line contact hole comprises the steps of:
4 forming a second liner on the substrate;
5 forming a first inter-layer dielectric layer on the
6 substrate to cover the second liner;
7 performing a chemical mechanical polishing process on
8 the first inter-layer dielectric, in which the
9 top of the first inter-layer dielectric is
10 leveled off with the top of the second liner;
11 forming a second inter-layer dielectric to cover the
12 first inter-layer dielectric and the second
13 liner;

14 providing a third photoresist layer having an opening
15 corresponding to the bit line contact hole; and
16 removing the second inter-layer dielectric and the
17 second liner exposed within the opening to expose
18 the top of the first conductive layer.

1 7. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the first liner
3 is removed before forming the second liner, thus the second
4 liner covers the first conductive layer, the first gate
5 conductive structure and the second gate conductive
6 structure.

1 8. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the second liner
3 is formed on top of the first conductive layer, thus the
4 combination of the first liner and the second liner covers
5 the first conductive layer, the first gate conductive
6 structure, and the second gate conductive structure.

1 9. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the second liner
3 is SiN or SiON.

1 10. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the thickness of
3 the second liner is 100~120Å.

1 11. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the first inter-
3 layer dielectric is a BPSG layer.

1 12. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the thickness of
3 the first inter-layer dielectric is 3500~3000Å.

1 13. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the second
3 inter-layer dielectric is a TEOS oxide layer.

1 14. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 6, wherein the thickness of
3 the second inter-layer dielectric is 3000~2500Å.

1 15. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 1, wherein the second
3 conductive layer is tungsten, polysilicon or other
4 conductive material.

1 16. A fabrication method for a damascene bit line
2 contact plug, comprising the steps of:

3 providing a semiconductor substrate having a first gate
4 conductive structure, a second gate conductive
5 structure, a third gate conductive structure and
6 a fourth gate conductive structure, in which the
7 second gate conductive structure and the third
8 gate conductive structure are formed within an
9 active area;

10 forming a first conductive layer to fill the space
11 between the second gate conductive structure and
12 the third gate conductive structure;

13 forming a liner on the substrate to cover the first
14 gate conductive structure, the second gate

15 conductive structure, the third gate conductive
16 structure and the fourth gate conductive
17 structure;
18 forming a first inter-layer dielectric to fill the
19 space between the first gate conductive structure
20 and the fourth gate conductive structure, and
21 fill the space between the second gate conductive
22 structure and the third gate conductive
23 structure;
24 forming a second inter-layer dielectric on the first
25 inter-layer dielectric;
26 forming a bit line contact hole, a gate contact hole
27 and a source contact hole, in which the bit line
28 contact hole exposes the top of the first
29 conductive layer, the gate contact hole exposes
30 the top of the first gate conductive structure,
31 and the source contact hole exposes the substrate
32 laterally adjacent to the fourth gate conductive
33 structure; and
34 forming a second conductive layer to fill the bit line
35 contact hole, the gate contact hole and the
36 source contact hole, in which the second
37 conductive layer formed in the bit line contact
38 hole is electrically connected to the first
39 conductive layer to serve as a damascene bit line
40 contact plug.

1 17. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 16, wherein the
3 semiconductor substrate further comprises a first shallow

4 trench isolation region and a second shallow trench
5 isolation region to define the active area, in which the
6 first shallow trench isolation region is formed between the
7 first gate conductive structure and the second gate
8 conductive structure, and the second shallow trench
9 isolation region is formed between the third gate conductive
10 structure and the fourth gate conductive structure.

1 18. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 16, wherein the
3 semiconductor substrate further comprises:

4 a first source/drain region formed in the substrate
5 between the second gate conductive structure and
6 the third gate conductive structure; and

1 a second source/drain region formed in the substrate
2 outside the active area and laterally adjacent to
3 the fourth gate conductive structure;

4 wherein, the first conductive layer is electrically
5 connected to the first source/drain region; and

6 wherein, the source contact hole exposes the second
7 source/drain region.

1 19. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 16, wherein the formation
3 of the bit line contact hole comprises the steps of:

4 forming a first liner on the substrate to cover the
5 first gate conductive structure, the second gate
6 conductive structure, the third gate conductive
7 structure and the fourth gate conductive
8 structure;

9 providing a first photoresist layer having an opening
10 corresponding to the bit line contact hole;
11 removing the first liner exposed within the opening to
12 expose the substrate between the second gate
13 conductive structure and the third gate
14 conductive structure;
15 removing the first photoresist layer;
16 depositing the first conductive layer to fill the space
17 between the second gate conductive structure and
18 the third gate conductive structure;
19 performing a chemical mechanical polishing process on
20 the first conductive layer, in which the top of
21 the first conductive layer is higher or
22 approximately equal to the first liner positioned
23 on top of the second gate conductive structure
24 and the third gate conductive structure;
25 providing a second photoresist layer having a pattern
26 corresponding to the bit line contact hole; and
27 removing the first conductive layer not covered by the
28 second photoresist layer, in which the first
29 conductive layer remains in the space between the
30 second gate conductive structure and the third
31 gate conductive structure.

1 20. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 19, wherein the formation
3 of the first conductive layer further comprises the steps
4 of:

1 removing the second photoresist layer; and

2 performing a wet etching process to remove polymer
3 residue from the substrate.

1 21. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 19, wherein the first liner
3 is SiN or SiON.

1 22. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 19, wherein the thickness
3 of the first liner is 100~120Å.

1 23. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 16, wherein the formation
3 of the bit line contact hole, the gate contact hole and the
4 source contact hole comprises the steps of:

5 forming a second liner on the substrate;

6 forming a first inter-layer dielectric layer on the
7 substrate to cover the second liner;

8 performing a chemical mechanical polishing process on
9 the first inter-layer dielectric, in which the
10 top of the first inter-layer dielectric is
11 leveled off with the top of the second liner;

12 forming a second inter-layer dielectric to cover the
13 first inter-layer dielectric and the second
14 liner;

15 providing a third photoresist layer having a first
16 opening corresponding to the bit line contact
17 hole, a second opening corresponding to the gate
18 contact hole, and a third opening corresponding
19 to the source contact hole; and

20 removing the second inter-layer dielectric, the first
21 inter-layer dielectric and the second liner
22 exposed within the first opening, the second
23 opening, and the third opening, thus exposing the
24 top of the first conductive layer, the top of the
25 first gate conductive structure and the substrate
26 laterally adjacent to the fourth gate conductive
27 structure.

1 24. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the first liner
3 is removed before forming the second liner, thus the second
4 liner covers the first conductive layer, the first gate
5 conductive structure, the second gate conductive structure,
6 the third gate conductive structure and the fourth gate
7 conductive structure.

1 25. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the second
3 liner is formed on top of the first conductive layer, thus
4 the combination of the first liner and the second liner
5 covers the first conductive layer, the first gate conductive
6 structure, the second gate conductive structure, the third
7 gate conductive structure and the fourth gate conductive
8 structure.

1 26. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the second
3 liner is SiN or SiON.

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1 27. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the thickness
3 of the second liner is 100~120Å.

1 28. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the first
3 inter-layer dielectric is a BPSG layer.

1 29. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the thickness
3 of the first inter-layer dielectric is 3500~3000Å.

1 30. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the second
3 inter-layer dielectric is a TEOS oxide layer.

1 31. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 23, wherein the thickness
3 of the second inter-layer dielectric is 3000~2500Å.

1 32. The fabrication method for a damascene bit line
2 contact plug as claimed in claim 16, wherein the second
3 conductive layer is tungsten, polysilicon or other
4 conductive material.